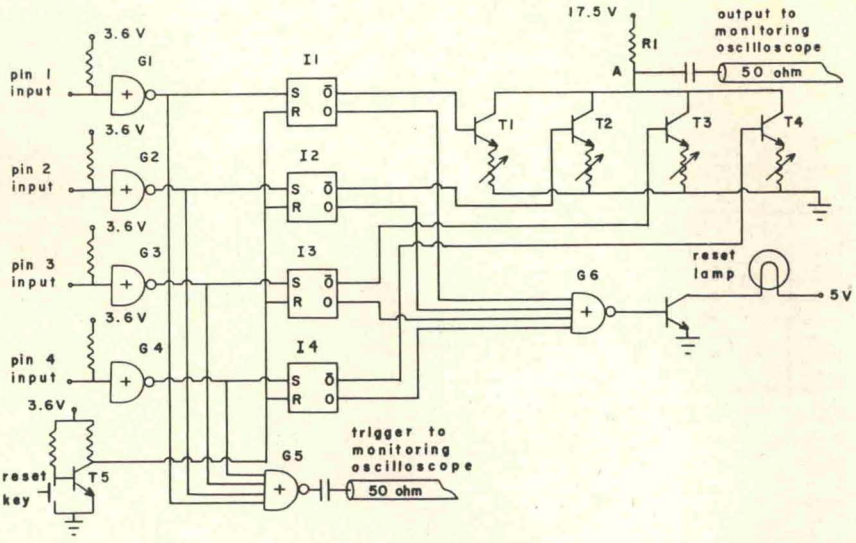

FIG. 17. Block schematic of velocity and tilt circuits.

are connected to the set terminals of gates I1, I2, I3, and I4, respectively. I1–I4 are properly designated as set–reset flipflops. It is the property of these gates that produces the set and reset modes in the circuit.

A set–reset flipflop is a bistable electronic device. A positive going pulse of amplitude greater than 0.7 V applied to the reset input will place the flipflop in reset state where it will remain until a positive pulse is applied to the set input. When a pulse is applied to the set input the device flips to the set state and remains there until again reset. The device has two outputs that will be designated here as 0 and $\bar{0}$.

When the reset key in the circuit is depressed a positive pulse from transistor T5 connected to the reset inputs of I1–I4 places the circuit in the reset mode. The 0 output of each flipflop is fed into G6, a four input nor gate, the output of which turns on a transistor to drive the reset lamp.

The $\bar{0}$ outputs of the set–reset flipflops I1, I4, I3, and I4 are connected to the base junctions of transistors T1, T2, T3, and T4, respectively. These transistors are then turned on when the circuit is in the reset mode. Each transistor acts as a current source and is connected to resistor Rl which sums the current from these four transistors. The variable resistor attached to the emitter of each transistor is used to adjust the current flowing through each transistor in order to provide the desired current ratios as previously mentioned.

The transistors T1–T4 then act as switches, either permitting or preventing the flow of current through resistor R1. These switches are all closed when the circuit is in the reset mode since all transistors will be held on by the $\bar{0}$ outputs of gates I1–I4. The voltage at point A in the circuit as shown in Fig. 17 will be, for the reset mode,

$$V_0 = 17.5 - 100(I_1 + I_2 + I_3 + I_4). \tag{2}$$

Now consider shorting input 1 of the circuit to ground. The voltage output of G1 will rise from 0 to 3.6 V. This positive pulse at the output of G1 flips I1 to the set position which turns off the reset lamp and turns off transistor T1. The voltage at point A will now be given by

$$V_1 = 17.5 - 100(I_2 + I_3 + I_4). \tag{3}$$

The voltage change at A appears as a step on the oscilloscope proportional to I_1, i.e.,

$$V_1 - V_0 = 100 I_1.$$

When input 1 is shorted to ground the positive pulse from the output of G1 also provides an input to G5 (a four input nor gate). This gate produces a negative going pulse which is used to trigger the monitoring oscilloscope.

Channels 2–4 all operate in the same manner as described above for channel 1. The complete circuit diagram for the velocity and tilt circuits is shown in Fig. 18.

The velocity circuit has one feature absent in the tilt circuit. Attached to each of channels 3 and 4 of the velocity circuit is a signal output circuit as shown in Fig. 18. When pin 3 or 4 is shorted, a negative pulse will appear at the respective auxiliary outputs. These outputs may be used to trigger external circuitry, i.e., manganin gauge current supplies, time interval counters, measurement oscilloscopes etc.

B. Quartz Gauge Calibration Circuit

The quartz gauge technique is used to measure pressure profiles during shock compression. Based upon the piezoelectric properties of quartz, this gauge produces a current that is proportional to the stress difference across the thickness of the quartz.[10] For pressures below 30 kilobars the current–stress relation is accurately known and for a given current observed from the gauge the stress difference may be computed. Consequently, it is necessary to calibrate the measurement oscilloscopes directly to establish an accurate

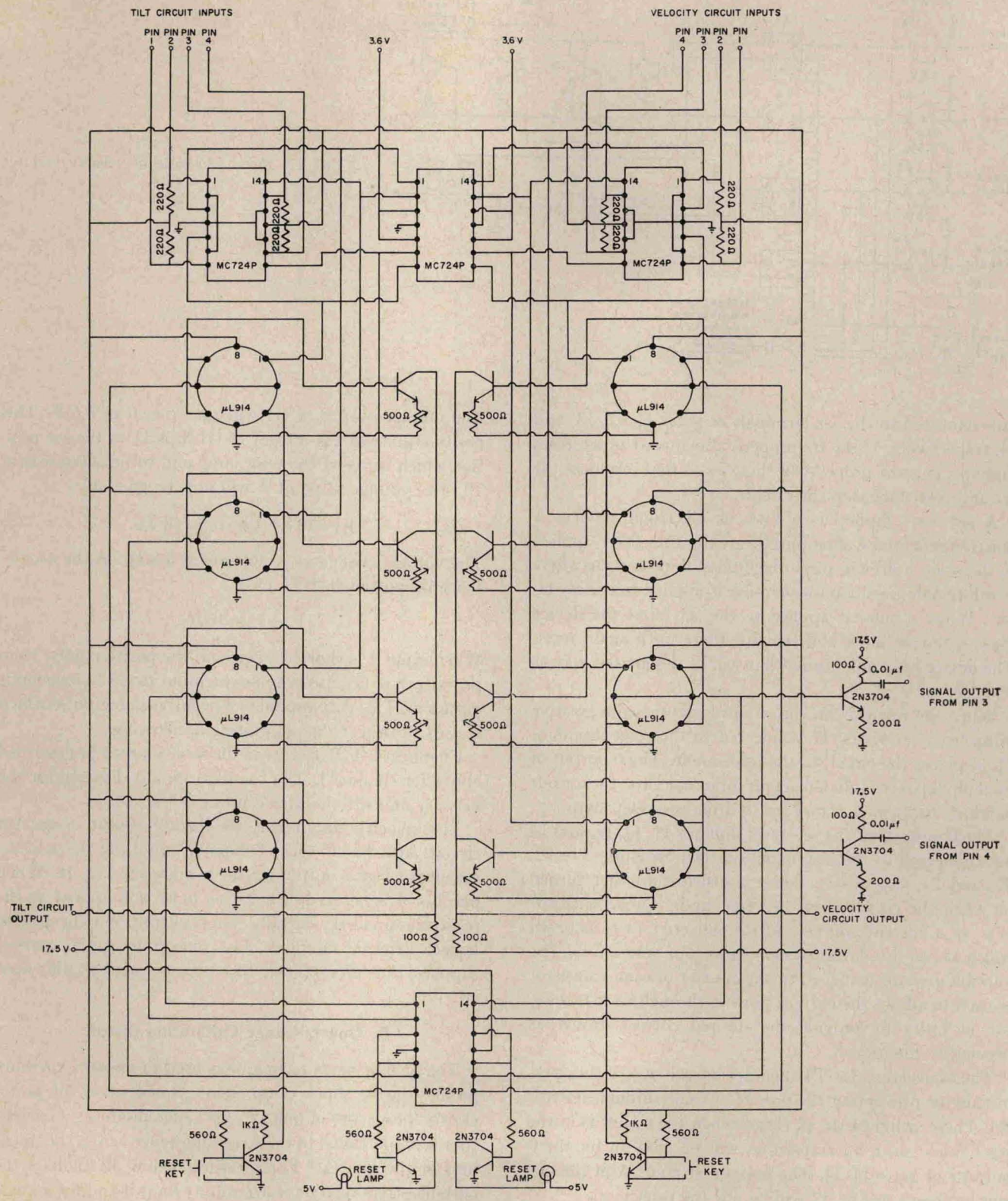

FIG. 18. Circuit diagram for velocity and tilt circuits.